CLAIMS

1. A delay element, comprising:

an input signal to be delayed; and

a series of at least one delay stage;

wherein each delay stage includes a stack of uniform minimum channel length transistors;

wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage;

wherein a drain of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage; and

wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage.

2. The delay element according to claim 1, wherein each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor;

wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a source of the last additional transistor is connected to a drain of the bottom transistor; and

wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack.

3. The delay element according to claim 1, wherein each transistor is a n-channel FET.

4 The delay element according to claim 1, wherein each transistor is a p-channel FET.

5. The delay element according to claim 2, wherein each transistor is a n-channel FET.

6. The delay element according to claim 2, wherein each transistor is a p-channel FET.

7. The delay element according to claim 1, wherein the input signal to be delayed is a clock signal.

8. The delay element according to claim2, wherein the input signal to be delayed is a clock signal.

9. A memory circuit comprising:

at least one delay element; wherein the delay element includes:

an input signal to be delayed; and

a series of at least one delay stage;

wherein each delay stage includes a stack of uniform minimum channel length transistors;

wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage;

wherein a drain of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage; and

wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage.

10. A clock circuit comprising:

at least one delay element, wherein each delay element includes:

an input signal to be delayed; and

a series of at least one delay stage;

wherein each delay stage includes a stack of uniform minimum channel length transistors;

wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage;

wherein a drain of a top transistor in the stack is coupled to a first reference voltage;

wherein a source of a bottom transistor in the stack is coupled to a second reference voltage; and

wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage.

11. A delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising:

a first transistor with a drain electrically coupled to a first reference voltage;

a last transistor with a source electrically coupled to a second reference voltage;

a totem pole of at least two transistors, the totem pole including:

a top transistor with a drain electrically coupled to a source of the first transistor;

a bottom transistor with a source electrically coupled to a drain of the last transistor; and

zero or more transistors, wherein the zero or more transistors complete the totem pole arrangement, wherein a drain of each of the zero or more transistors is electrically coupled to a source of an adjacent transistor within the zero or more transistors relative to the each of the zero or more transistors, and wherein each of the transistors within the totem pole comprise a minimum channel length transistor;

an input electrically coupled to each gate within the totem pole; and

an output electrically coupled to connection between one source and one drain of two transistors within the totem pole.

12. The delay circuit according to claim 11, wherein each transistor is a p-channel FET.

13. The delay circuit according to claim 11, wherein each transistor is a n-channel FET.

14. The delay circuit according to claim 11, wherein the input signal to be delayed is a clock signal.